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HEWLETT-PACKARD COMPANY
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PATENT APPLICATION

ATTORNEY DOCKET NO. 200313420-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

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| Inventor(s): | Brad Underwood et al. | Confirmation No.: | 4159 |
| Application No.: | 10/797,776 | Examiner: | Luu, An T |
| Filing Date: | 03/10/2004 | Group Art Unit: | 2816 |

Title: SYSTEM AND METHOD FOR PROVIDING DISTRIBUTED CONTROL SIGNAL REDUNDANCY AMONG ELECTRONIC CIRCUITS

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

## TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on 01/17/2006.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

**(complete (a) or (b) as applicable)**

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

| | | | |
|---|---|---|---|
| ☐ 1st Month $120 | ☐ 2nd Month $450 | ☐ 3rd Month $1020 | ☐ 4th Month $1590 |

☐ The extension fee has already been filed in this application.

☐ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 500. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

(X) I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV482725455US, in an envelope addressed to: MS Appeal Brief, Director for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: 03/13/2006

OR

☐ I hereby certify that this paper is being transmitted to the Patent and Trademark Office facsimile number (571)273-8300.

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Respectfully submitted,

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Docket No.: 200313420-1
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:
Brad Underwood et al.

Application No.: 10/797,776 | Confirmation No.: 4159

Filed: March 10, 2004 | Art Unit: 2816

For: SYSTEMS AND METHODS FOR PROVIDING DISTRIBUTED CONTROL SIGNAL REDUNDANCY AMONG ELECTRONIC CIRCUITS | Examiner: A. T. Luu

## APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under 37 C.F.R § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on January 17, 2006, and is in furtherance of said Notice of Appeal.

The fees required under 37 C.F.R § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205.02:

| | |
|---|---|
| I. | Real Party In Interest |
| II. | Related Appeals and Interferences |
| III. | Status of Claims |
| IV. | Status of Amendments |
| V. | Summary of Claimed Subject Matter |
| VI. | Grounds of Rejection to be Reviewed on Appeal |

## I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Hewlett-Packard Development Company, L.P., a Texas Limited Partnership having its principal place of business in Houston, Texas.

## II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

## III. STATUS OF CLAIMS

### A. Total Number of Claims in Application

There are 28 claims pending in application.

### B. Current Status of Claims

1. Claims canceled: 0
2. Claims withdrawn from consideration but not canceled: 0
3. Claims pending: 28
4. Claims allowed: 0
5. Claims rejected: 1-28

### C. Claims On Appeal

The claims on appeal are claims 1-28.

## IV. STATUS OF AMENDMENTS

Appellant did not file an Amendment After Final Rejection. The claims enclosed herein as Appendix A include amendments made filed by Appellant on September 6, 2005, and indicated as entered by the Final Office Action, dated November 2, 2005 ("Final Action").

Appendix A also includes an amendment to claim 26 to correct obvious an typographical errors. This correction changes the dependency of claim 26 from claim 21 to claim 23. Claim 26 is also amended to more clearly define the invention. The term "second node" on line 5 is changed the "third node," "first output" on line 7 is changed to "third output" and "second input" on line 8 is changed to "input of the first node." Appellant asserts that support for these amendments can be found in the originally-filed application, at least, in Figure 5. These amendment were not made earlier, because the need for these corrections was not noticed until now. These amendments simplify issues for appeal, and do not add any new matter.

## V. SUMMARY OF CLAIMED SUBJECT MATTER

According to claim 1, a distributed redundant control signal distribution system (item 10) comprises: a first control signal source (item 11) co-located with a first set of control signal controlled circuit elements (items 16-01 and 16-0N); at least one second control signal source (item 12) co-located with a second set of control signal controlled circuit elements (items 16-11 16-1N); a first controller (items 17-0 and 13-0); and at least one second controller (items 17-1 and 13-1); said first controller and second controller operable for substituting signals from said second control signal source for signals from said first control signal source if said signals from said first control signal source become unavailable to either said first or second circuit elements (page 3, paragraph [0012], line 1 through paragraph[0013], line 4; Fig. 6). (All referenced items appear at least in Figures 1 and 2.)

According to claim 3, first and second sets of circuit elements (items 16-01, 16-0N, 16-11 and 16-1N); are interconnected by at least two transmission paths (items 101 and 102), wherein controlling signals travel over both of said transmission paths (page 2, paragraph [0010], lines 7-9). (All referenced items appear at least in Figures 1 and 2.)

According to claim 12, a method (see Fig. 6) for distributing control signals among a plurality of electronic boards (items BP0 and BP1), each electronic board having associated therewith control signal controlled circuitry (items 16-01, 16-0N, 16-11 and 16-1N), comprises: accepting, on each of said plurality of electronic boards, control signals originating from a first and second one of said electronic boards (page 2, paragraph [0010], lines 1-3); and on each said first and second board hierarchically controlling said control signals such that either of said control signals originating from said first or from said second electronic boards are operative to control said controlled signal controlled circuitry on all of said electronic boards (page 3, paragraph [0012], lines 2-8). (All referenced items appear at least in Figures 1 and 2.)

According to claim 16, a system for controlling clock signals for a plurality of electronic boards (item 10) comprises: a clock source (items 11 and 12) on at least two of said electronic boards (items BP0 and BP1); at least one signal connection between all of said electronic boards (items 101 and 102), each said signal connection allowing clock signals to pass between said plurality of boards (page 2, paragraph [0010], lines 7-9); a controller on each of said boards (items 17-0, 13-0, 17-1 and 13-1), said controller operable for hierarchically selecting clock signals from at least one of said signal connections (page 3, paragraph [0012], lines 2-8); and wherein said signal controllers on said first and second electronic boards are further operable for hierarchically selecting one or the other of said clock sources (page 3, paragraph [0012], lines 2-8). (All referenced items appear at least in Figures 1 and 2.)

According to claim 20, a method (see Fig. 6) for protecting electronic circuits (items BP0 and BP1) from dual clocking signal failures comprises: interconnecting said electronic circuits with dual independent clock (items 11 and 12) signal transmission facilities (items 101 and 102; page 2, paragraph [0011], lines 1-2); providing to the input of a controller on each electronic circuit (items 17-0, 13-0, 17-1 and 13-1) a clock signal generated local to said controller (items 11, 17-0 and 13-0 are all on BP0 and items 12, 17-1 and 13-1 are all on BP1), the output of said controller supplying clock signals for circuitry local to said controller (items 16-01 and 16-0N on BP0 and items 16-11 and 16-1N on BP1), said output further supplying clock signals as inputs to said dual independent transmission facilities; providing to

said input of said controller, clock signals from each of said signal transmission facilities; and hierarchically selecting one of said inputs for presentation of the signals on said selected input to said output of said controller (page 3, paragraph [0012], lines 2-8). (All referenced items appear at least in Figures 1 and 2.)

According to claim 21, a distributed redundant control signal distribution system (item 10) comprises: a first system node (item BP0), comprising a control signal source (item 11), a controller (items 17-0 and 13-0), an input (B and C of item 102; page 3, paragraph [0011], lines 5-6), an output (page 2, paragraph [0010], lines 7-9) and a first set of circuit elements requiring a control signal (items 16-01 and 16-0N); and a second system node (item BP1), comprising a control signal source (item 12), a controller (items 17-1 and 13-1), an input ((B and C of item 101; page 2, paragraph [0010], lines 7-9), an output (page 3, paragraph [0011], lines 3-6) and a second set of circuit elements requiring a control signal (items 16-11 and 16-1N); wherein the output of the first node is coupled to the input of the second node (page 2, paragraph [0010], lines 7-9); wherein the output of the second node is coupled to the input of the first node (page 3, paragraph [0011], lines 3-6); and wherein the controller of the first node operates in tandem with the controller of the second node to alternatively select between the control signal sources of the first and second node to supply a control signal to the first set and second set of circuit elements (see entirety of paragraph [0015] on pages 3 and 4). (All referenced items appear at least in Figures 1 and 2.)

According to claim 24, a third node of a distributed redundant control signal distribution system (item 50) further comprises: a third set of circuit elements requiring a control signal (items 16-21 and 16-2N); wherein the third set of circuit elements requiring a control signal receives the same signal as both the first and second sets of circuit elements requiring a control signal (items 16-01, 16-0N, 16-11 and 16-1N). (All referenced items appear in Figure 5.)

According to claim 25, a third node of a distributed redundant control signal distribution system (item 50) further comprises: a third control signal source (page 4, paragraph [0019], line 5); wherein the first, second and third controllers (items 17-0, 13-0, 17-1, 13-1, 17-2 and 13-2) operate in tandem to select among the first, second and third

control signal sources for supplying to the sets of circuit elements requiring a control signal. (All referenced items appear in Figure 5.)

According to claim 26, a distributed redundant control signal distribution system (item 50) further comprises: a fourth system node (BPN), comprising a fourth controller (items 17-N and 13-N), a fourth input (items B and C of 503) and a fourth output (output of item 13-N); wherein the first node (BP0) is coupled to the third node (BP2) through the fourth node; wherein the third output (output of item 13-2) is coupled to the fourth input; wherein the fourth output is coupled to the input of the first node (items B and C of 102 at BP0); and wherein the first, second, third and fourth controllers operate in tandem to select among the first and second control signal sources for supplying to the sets of circuit elements requiring a control signal.

According to claim 27, the first controller (items 17-0 and 13-0) and second controller (items 17-1 and 13-1) of a distributed redundant control signal distribution system (item 10) each comprises a multiplexer (items 13-0 and 13-1) for accepting multiple signals (items A, B, C and D) at the inputs of the multiplexer and selecting which one of the signals is passed to the output of the multiplexer (page 3, paragraph [0012], line 1 through paragraph[0013], line 4; Fig. 6). (All referenced items appear at least in Figures 1 and 2.)

## VI. GROUNDS OF OBJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-28 properly stand rejected under 35 U.S.C. § 112, second paragraph.

Whether claims 1-5, 7-8, 12-18, 20-22, 27 and 28 properly stand rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 6,194,969 to Doblar ("Doblar").

## VII. ARGUMENT

### A. First Ground of Rejection

The Final Action indicates that claims 1-28 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to point out and distinctly claim the subject

matter which the Appellant regards as the invention. Specifically, the Examiner asserts that claims 1, 3 and 20 each have a lack of antecedent basis; claims 21 and 24-26 have unclear limitations; claim 26 has a lack of antecedent basis for the term "fourth," because there is no "third;" and claim 27 has both a limitation that is not understood and a lack of antecedent basis. Claims 2, 4-11, 22, 23 and 28 stand rejected under 35 U.S.C. § 112 merely due to dependence from a rejected claim. Appellant notes that no basis for rejection of claims 12-19 is provided by the Final Action. Further, Appellant notes that if the scope of a claim would be reasonably ascertainable by those skilled in the art, then the claim is not indefinite. *Ex parte Porter*, 25 USPQ2d 1144, 1145 (Bd. Pat. Appl & Inter. 1992).

1. Independent Claim 1 and Dependent Claims 2 and 5-11

The Final Action asserts that the limitation "signals" in lines 10 and 11 of claim 1 lacks antecedent basis, and that it appears that each signal source provides a only single signal. The rejections of claims 2 and 5-11 result from dependence from claim 1. Appellant asserts that claim 1 does not limit each signal source to providing only a single signal. For example, claim 1 recites "a first control signal source co-located with a first set of control signal controlled circuit elements ...." Appellant asserts that there is no limitation for the first control signal source to provide only a single signal. Accordingly, Appellant requests that the 35 U.S.C. § 112, second paragraph, rejections of claims 1, 2 and 5-11 be reversed.

2. Dependent Claims 3 and 4

The Final Action asserts that the limitation "said controlling signals" in lines 2 and 3 of claim 3 lacks antecedent basis. The rejection of claim 4 results from its dependence from claims 3 and 1. Appellant asserts that one of skill in the art would understand that "said controlling signals" are signals from the control signal sources recited in claim 1. Therefore, the scope of claim 3 would be reasonably ascertainable by those skilled in the art, and claim 3 is not indefinite. Accordingly, Appellant requests that the 35 U.S.C. § 112, second paragraph, rejections of claims 3 and 4 be reversed.

3. Independent Claim 12 and Dependent Claims 13-19

The Final Action does not provide any basis for rejection of claims 12-19. Appellant therefore asserts that the rejections of claims 12-19 are improper. Accordingly, Appellant requests that the 35 U.S.C. § 112, second paragraph, rejections of claims 12-19 be reversed.

4. Independent Claim 20

The Final Action asserts that the limitation "signals" in claim 20 lacks antecedent basis, but gives only the explanation "the same issue as that of claim 1." Appellant interprets this to mean that the Examiner reads claim 20 to include a limitation that only a single signal is provided. Appellant notes that the term "signals" appears four times in claim 20, and the first occurrence is on line 6. Appellant further notes that claim 20 recites "the output of said controller supplying clock signals." That is, claim 20 specifically recites that a controller may provide signals, rather than just a single signal. Therefore, Appellant asserts that the limitation "signals" does not lack antecedent basis, and requests that the 35 U.S.C. § 112, second paragraph, rejection of claim 20 be reversed.

5. Independent Claim 21 and Dependent Claims 22 and 23

The Final Action asserts that it is unclear whether the limitation "a control signal" in line 15 of claim 21 is related to that of lines 4-5 and 7-8. The rejections of claims 22 and 23 result from dependence from claim 1. Appellant asserts that, based upon the usage of the phrase "a control signal" in lines 4-5 and 7-8 of claim 21, the introduction of "a control signal" in line 15 with an indefinite article is proper and is not unclear. Appellant notes that lines 4-5 of claim 21 do not recite that "a control signal" is supplied – only that "a control signal" is required by a first set of circuit elements. Lines 7-8 recite a similar requirement for a second set of control circuit elements. Therefore, Appellant asserts that one skilled in the art would reasonably ascertain that "supply a control signal to the first and second set of circuit elements" in lines 15-16 satisfies "circuit elements requiring a control signal" recited in lines 4-5 and 7-8. Accordingly, Appellant requests that the 35 U.S.C. § 112, second paragraph, rejections of claims 21-23 be reversed.

6. Dependent Claim 24

The Final Action asserts that the limitation "a control signal" in claim 24 has "the same issue as noted in claim 21." Appellant notes that claim 24 merely recite the need for control signals, and repeats a limitation with proper antecedent basis in claim 21. For example, claim 24 recites "a third set of circuit elements requiring a control signal ...." Claim 24 further recites that "the third set of circuit elements requiring a control signal receives the same signal as both the first and second sets of circuit elements requiring a control signal."

Appellant asserts that one skilled in the art would reasonably ascertain that "supply a control signal to the first and second set of circuit elements" in claim 21 satisfies "circuit elements requiring a control signal" recited in line 3 of claim 24. Appellant further asserts that the recitations of "a control signal" in lines 4-5 and 6 of claim 24 are clear in light of the antecedent basis provided for "circuit elements requiring a control signal" given in claims 21 and 24. Accordingly, Appellant requests that the 35 U.S.C. § 112, second paragraph, rejections of claim 24 be reversed.

7. Dependent Claim 25

The Final Action asserts that the limitation "a control signal" in claim 25 has "the same issue as noted in claim 21." Appellant notes that claim 25 merely repeats a phrase with a proper antecedent from claim 21. Accordingly, Appellant requests that the 35 U.S.C. § 112, second paragraph, rejection of claim 25 be reversed.

8. Dependent Claim 26

The Final Action asserts that the limitation "a control signal" in claim 26 has "the same issue as noted in claim 21," and that the limitation "a fourth system node" lacks antecedent basis because there is no "third system node." Appellant notes that "a control signal" has a proper antecedent from claim 21. Appellant has corrected an obvious typographical error. Claim 26 now depends from claim 23, which recites a "third system node." Accordingly, Appellant requests that the 35 U.S.C. § 112, second paragraph, rejection of claim 26 be reversed.

9. Dependent Claims 27 and 28

The Final Action asserts that the limitation "multiple signals" in claim 27 is not understood since it is inherent that a MUX receives multiple input signals, and also that "the signals" on line 3 lacks antecedent basis. The rejection of claim 28 results from its dependence from claims 27 and 21. Appellant disagrees that a MUX inherently receives multiple input signals, and asserts that many multiplexers could operate with only a single input signal. Further, Appellant asserts that the limitation "a multiplexer for accepting multiple signals" would be reasonable understood by one skilled in the art. Antecedent basis for "the signals" recited in line 4 of claim 27 is provided by "multiple signals" in line 3 of claim 27. Accordingly, Appellant requests that the 35 U.S.C. § 112, second paragraph, rejections of claims 27 and 28 be reversed.

B. Second Ground of Rejection

Claims 1-5, 7-8, 12-18, 20-22, 27 and 28 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Doblar. To anticipate a claim under 35 U.S.C. § 102, a reference must teach every element of the claim. *See* M.P.E.P. § 2131. Moreover, in order for an applied reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim." *See* M.P.E.P. § 2131 (citing *Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q.2d 1913 (Fed. Cir. 1989). As discussed below, Doblar fails to teach every element of the claims to which it is applied, and further, does not show the identical invention in as complete detail as is contained in the claims.

1. Independent Claim 1 and Dependent Claims 2-5, 7 and 8

Claim 1 recites "at least one second controller; said first controller and second controller operable for substituting signals ...." Doblar does not disclose at least this element of claim 1. That is, Doblar does not disclose a second controller that operates with a first controller to substitute control signals. The Final Action points to controller 110 of Doblar, along with column 3, lines 31-32 of Doblar, which states "a portion of the system controller 110 may be located on each board." Since Figure 1 of Doblar shows two clock boards 105,

the Final Action alleges that Doblar "clear[ly] teaches a first controller and a second controller."

However, rather than disclosing two controllers, Doblar merely discloses that a single controller may be split between boards. Appellant notes that a single controller with portions located on separate boards is not two controllers as defined by claim 1. Therefore, Doblar does not disclose at least one second controller, wherein a first controller and the second controller are operable for substituting signals, as required by the claim. Accordingly, Appellant respectfully requests withdrawal of the 35 U.S.C. § 102(b) rejection of claim 1.

Claims 2-5, 7 and 8 depend from claim 1 and are patentable for at least the same reasons as independent claim 1. Therefore, Appellant also respectfully requests withdrawal of the 35 U.S.C. § 102(b) rejections of claims 2-5, 7 and 8.

2. Independent Claim 12 and 13-15

Claim 12 recites "on each said first and second board hierarchically controlling said control signals ...." Doblar does not disclose at least this aspect of claim 12. That is, Doblar does not disclose hierarchical control on each of two separate boards. The Final Action references the rejection of claim 1.

However, rather than disclosing two boards, each with hierarchical control, Doblar merely discloses that a single controller may be split between boards. Doblar, column 3, lines 31-32. Appellant notes that a single controller with portions located on separate boards is not hierarchical control on each of two boards as defined by claim 12. Therefore, Doblar does not disclose all the limitations of claim 12.

Accordingly, Appellant respectfully requests withdrawal of the 35 U.S.C. § 102(b) rejection of claim 12. Claims 13-15 depend from claim 21 and are patentable for at least the same reasons as independent claim 12. Therefore, Appellant also respectfully requests withdrawal of the 35 U.S.C. § 102(b) rejections of claims 13-15.

3. Independent Claim 16 and Dependent Claims 17 and 18

Claim 16 recites "a controller on each of [at least two] boards ...." Doblar does not disclose at least this aspect of claim 16. That is, Doblar does not disclose at least two controllers, each on separate boards. The Final Action points to controller 110 of Doblar, which Doblar discloses may have a portion on each board, and alleges that this meets the requirement for a controller on each board. Doblar, column 3, lines 31-32.

However, rather than disclosing two controllers, Doblar merely discloses that a single controller may be split between boards. Appellant notes that a single controller with portions located on separate boards is not multiple controllers, one on each of multiple boards, as defined by claim 1. Therefore, Doblar does not disclose all the limitations of claim 16.

Accordingly, Appellant respectfully requests withdrawal of the 35 U.S.C. § 102(b) rejection of claim 16. Claims 17 and 18 depend from claim 16 and are patentable for at least the same reasons as independent claim 16. Therefore, Appellant also respectfully requests withdrawal of the 35 U.S.C. § 102(b) rejections of claims 17 and 18.

4. Independent Claim 20

Claim 20 recites "interconnecting said electronic circuits ... [and] providing to the input of a controller on each electronic circuit a clock signal generated local to said controller" Doblar does not disclose at least this aspect of claim 20. Appellant notes that the phrase "electronic circuits" is plural, so that the limitation "a controller on each electronic circuit" requires plural controllers. Doblar does not disclose plural controllers. As discussed above, Doblar merely discloses that a single controller may have portions located on separate boards. Doblar, column 3, lines 31-32.

Appellant asserts that a single controller with portions split between separate boards is not multiple controllers, each on separate boards, as defined by claim 20. Therefore, Doblar does not disclose all the limitations of claim 20. Accordingly, Appellant respectfully requests withdrawal of the 35 U.S.C. § 102(b) rejection of claim 20.

5. Independent Claim 21 and Dependent Claims 22, 77 and 28

Claim 21 recites "wherein the controller of the first node operates in tandem with the controller of the second node ...." Doblar does not disclose at least this element of claim 21. That is, Doblar does not disclose two controllers operating in tandem. As shown above, Doblar merely discloses that a single controller may have portions located on separate boards. Doblar, column 3, lines 31-32.

Appellant asserts that a single controller with portions split between separate boards is not two controllers operating in tandem, as defined by claim 21. Therefore, Doblar does not disclose all the limitations of claim 21.

Accordingly, Appellant respectfully requests withdrawal of the 35 U.S.C. § 102(b) rejection of claim 21. Claims 22, 27 and 28 depend from claim 21 and are patentable for at least the same reasons as independent claim 21. Therefore, Appellant also respectfully requests withdrawal of the 35 U.S.C. § 102(b) rejections of claims 22, 27 and 28.

## VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A include the amendments filed by Appellant on September 6, 2005 and one amendment currently made to claim 26.

## IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

## X. RELATED PROCEEDINGS

No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

Dated: March 13, 2006

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV482725455US, in an envelope addressed to: MS Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.

Dated: March 13, 2006

Signature: _____
Phyllis Ewing

Respectfully submitted,

By _____
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Attorney for Applicant

## APPENDIX A

**Claims Involved in the Appeal of Application Serial No. 10/797,776**

1. (Previously Presented) A distributed redundant control signal distribution system, said control system comprising:

a first control signal source co-located with a first set of control signal controlled circuit elements;

at least one second control signal source co-located with a second set of control signal controlled circuit elements;

a first controller; and

at least one second controller; said first controller and second controller operable for substituting signals from said second control signal source for signals from said first control signal source if said signals from said first control signal source become unavailable to either said first or second circuit elements.

2. (Original) The system of claim 1 wherein said control signal sources are system clocks.

3. (Original) The system of claim 1 wherein said first and second sets of circuit elements are interconnected by at least two transmission paths and wherein said controlling signals travel over both of said transmission paths.

4. (Previously Presented) The system of claim 3 wherein said first controller and at least one second controller enable said controlling signals to control both sets of controlled circuit elements even when one of said transmission paths is inoperative.

5. (Previously Presented) The system of claim 1 wherein said first controller and at least one second controller comprise a first multiplexer and a second multiplexer for accepting signals on their inputs from said first and second control signal sources, said first and second multiplexers operable for selecting which one of said control signals controls said controlled circuit elements.

6. (Previously Presented) The system of claim 5 wherein said first and second multiplexers have a preset hierarchical control among their respective inputs.

7. (Previously Presented) The system of claim 5 wherein said first multiplexer is co-located with said first set of controlled circuit elements.

8. (Previously Presented) The system of claim 7 wherein said second multiplexer is co-located with said second set of controlled circuit elements.

9. (Previously Presented) The system of claim 1 further comprising at least a third set of control signal controlled circuit elements wherein signals from said first control signal source control said third set of controlled circuit elements, said third set of controlled circuit elements having co-located therewith a controller for substituting signals from said second control signal source for said signals from said first signal control source if said signals from said first signal control source become unavailable.

10. (Original) The system of claim 9 wherein said last-mentioned controller comprises a multiplexer for accepting on its input a redundant set of control signals, said multiplexer operable for selecting which one of said redundant set of control signals controls said third set of controlled circuit elements.

11. (Original) The system of claim 10 wherein said at least one controller comprises a second multiplexer co-located with said first set of controlled circuit elements for accepting on its input said first and second control signals, said second multiplexer operable for selecting which one of the control signals control said first set of controlled circuit elements; and

wherein said at least one controller further comprises a third multiplexer co-located with said second set of controlled circuit elements for accepting on its input said first and second control signals, said third multiplexer operable for selecting which one of said control signals controls said second set of controlled circuit elements.

12. (Previously Presented) A method for distributing control signals among a plurality of electronic boards, each electronic board having associated therewith control signal controlled circuitry, said method comprising;

accepting, on each of said plurality of electronic boards, control signals originating from a first and second one of said electronic boards; and

on each said first and second board hierarchically controlling said control signals such that either of said control signals originating from said first or from said second electronic boards are operative to control said controlled signal controlled circuitry on all of said electronic boards.

13. (Original) The method of claim 12 wherein said electronic boards are interconnected with redundant connections; and

wherein said hierarchically control signals are switched from a first to a second connection upon detection of a lack of a control signal on said first connection.

14. (Original) The method of claim 13 wherein said hierarchical control is operable for allowing said control signals originating from said first electronic board to dominate, followed by control signals originating from said second electronic board.

15. (Original) The method of claim 13 wherein on said second electronic board said hierarchy control allows signals originating on said first electronic board and provided to said second electronic board over a pair of transmission links to dominate over said control signals originating on said second electronic board.

16. (Original) A system for controlling clock signals for a plurality of electronic boards, said system comprising:

a clock source on at least two of said electronic boards;

at least one signal connection between all of said electronic boards, each said signal connection allowing clock signals to pass between said plurality of boards;

a controller on each of said boards, said controller operable for hierarchically selecting clock signals from at least one of said signal connections; and

wherein said signal controllers on said first and second electronic boards are further operable for hierarchically selecting one or the other of said clock sources.

17. (Original) The system of claim 16 wherein the hierarchy is such that said controllers only select the clock source from said second one of said boards when the clock source from said first one of said boards is not available.

18. (Original) The system of claim 17 wherein said controllers are multiplexers.

19. (Original) The system of claim 16 wherein said at least one signal connector is a plurality of independent transmission paths; and

wherein said controllers accept signals from each of said transmission paths for said hierarchical selection.

20. (Original) A method for protecting electronic circuits from dual clocking signal failures, said method comprising:

interconnecting said electronic circuits with dual independent clock signal transmission facilities;

providing to the input of a controller on each electronic circuit a clock signal generated local to said controller, the output of said controller supplying clock signals for circuitry local to said controller, said output further supplying clock signals as inputs to said dual independent transmission facilities;

providing to said input of said controller, clock signals from each of said signal transmission facilities; and

hierarchically selecting one of said inputs for presentation of the signals on said selected input to said output of said controller.

21. (Previously Presented) A distributed redundant control signal distribution system, said system comprising:

a first system node, comprising a control signal source, a controller, an input, an output and a first set of circuit elements requiring a control signal; and

a second system node, comprising a control signal source, a controller, an input, an output and a second set of circuit elements requiring a control signal;

wherein the output of the first node is coupled to the input of the second node;

wherein the output of the second node is coupled to the input of the first node; and

wherein the controller of the first node operates in tandem with the controller of the second node to alternatively select between the control signal sources of the first and second node to supply a control signal to the first set and second set of circuit elements.

22. (Previously Presented) The system of claim 21 wherein said control signal sources are system clocks.

23. (Previously Presented) The system of claim 21 further comprising:

a third system node, comprising a third controller, a third input and a third output;

wherein the second node is coupled to the first node through the third node;

wherein the second output is coupled to the third input;

wherein the third output is coupled to the first input; and

wherein the first, second and third controllers operate in tandem to select among the first and second control signal sources for supplying to the first set and second set of circuit elements.

24. (Previously Presented) The system of claim 23 wherein the third node further comprises:

a third set of circuit elements requiring a control signal;

wherein the third set of circuit elements requiring a control signal receives the same signal as both the first and second sets of circuit elements requiring a control signal.

25. (Previously Presented) The system of claim 23 wherein the third node further comprises:

a third control signal source;

wherein the first, second and third controllers operate in tandem to select among the first, second and third control signal sources for supplying to the sets of circuit elements requiring a control signal.

26. (Currently Amended) The system of claim [[21]] 23 further comprising:

a fourth system node, comprising a fourth controller, a fourth input and a fourth output;

wherein the first node is coupled to the ~~second~~ third node through the fourth node;

wherein the ~~first~~ third output is coupled to the fourth input;

wherein the fourth output is coupled to the ~~second~~ input of the first node; and

wherein the first, second, third and fourth controllers operate in tandem to select among the first and second control signal sources for supplying to the sets of circuit elements requiring a control signal.

27. (Previously Presented) The system of claim 21 wherein the first controller and second controller each comprises a multiplexer for accepting multiple signals at the inputs of the multiplexer and selecting which one of the signals is passed to the output of the multiplexer.

28. (Previously Presented) The system of claim 27 wherein the multiplexer has a preset hierarchical control among its respective inputs.

## APPENDIX B

**Evidence: None**

## APPENDIX C

**Related Proceedings: None**